Customer No.: 31561
Docket No.: 500-002
Application No.: 10/630,983

REMARKS

Present Status of the Application

The final Office Action rejected claims 7-14 under 35 U.S.C. 112, first paragraph and rejected claims 13-14 under 35 U.S.C. 112, second paragraph. Claims 1-3, 5 and 6 are rejected under 35 U.S.C 103(a) as being unpatentable over Gans et al. (US 6,353,521 and Gans hereinafter) in view of Konno (US 5,914,516, and Konno hereinafter). Claim 4 is rejected under 35 U.S.C 103(a) as being unpatentable over Gans in view of Konno, and further in view of the admitted prior art , Fig. 1 in the present application. Claims 7-12 are rejected under 35 U.S.C 103(a) as being unpatentable over Kim (US 6,724,226 and Kim hereinafter) in view of Konno. Patentability of claims 13-14 cannot be determined because of indefiniteness. Reconsideration and allowance of those claims are respectfully requested.

Discussion of Claim Rejection under 35 USC 112, first paragraph

The final Office Action rejected claims 7-14 under 35 U.S.C. 112, first paragraph. Applicant respectfully disagrees and traverses the above rejection as set forth below.

The previously added and currently amended limitation "said transition circuit comprising with a Pch MOS transistor and a Nch MOS transistor; the source of said Pch MOS transistor and the Nch MOS transistor being coupled with the input of said transition circuit; the drain of said Pch MOS transistor and the Nch MOS transistor being coupled with the output of said transition circuit; the gate of said Pch MOS transistor being coupled with a third voltage source; the gate of said Nch MOS transistor being coupled with a fourth voltage source." ***is not New Matter***

because the limitation is recited and supported in Fig. 3 and lines 1-11, page 6 of the originally filed application. The Pch MOS and Nch transistors are, for example but not limited by, the PMOS transistor 311 and the NMOS transistor 312 in Fig. 3.

Discussion of Claim Rejection under 35 USC 112, first paragraph

The final Office Action rejected claims 13-14 under 35 U.S.C. 112, second paragraph. Applicants amended claim 13 to overcome this rejection. Besides, it is advised that claim 14 is dependent on claim 12, not claim 13.

Discussion of Rejection on Claims 1-6 under 35 USC 103(a)

The final Office Action rejected claims 1-3, 5 and 6 under 35 U.S.C. 103(a) as being unpatentable over Gans in view of Konno.

Applicant respectfully disagrees and traverses the above rejection as set forth below.

The combination of Gans's voltage protection circuit with Konno's two capacitors is submitted to be improper because neither Gans nor Konno suggests such a combination and one skilled in the art would have no motivation to make such a combination.

Besides, even if the combination could be made, claim 1 distinguishes because the combination does not disclose, teach, or suggest, either implicitly or explicitly, all elements/features of claim 1.

Gans's voltage protection circuit cannot be used as an inverter. An inverter inverts a logic high signal to a logic low signal and vice versa. In Gans, during an ESD event in which a high potential applies, transistors 15 or 20 actuates to reduce the potential at node 30 to less than the high potential, and this potential reduce by transistors 15 or 20 cannot be seemed as a "high-to-low invert" because the potential at node 30 is decreased to a value below the high potential, not exactly "inverted to a logic low". (See Gans's column 3, lines 29-37). Secondly, the voltage protection circuit of Gans cannot invert a logic low signal to a logic high signal because during normal operation in which, for example, a low potential applies, transistors 15 and 20 are deactivated and most importantly, that the potential at node 30 is determined by the potential at bond pad 25 and the resistor 10, not inverted by transistors 15 and 20. (See Gans's column 3, lines 38-42 and FIG. 2). So, it is concluded that the voltage protection circuit in Gans cannot be used as an inverter because voltage protection circuit cannot invert a logic high signal to a logic low signal and a logic low signal to a logic high signal.

Consequently, the combination of Gans in view of Konno does not render claim 1 obvious, and the rejection should be withdrawn.

Because independent claim 1 are allowable over the prior art of record, its dependent claim 2-6 are allowable as a matter of law, for at least the reason that the dependent claims contain all features/elements of their respectively independent claims.

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Discussion of Rejection on Claims 7-12 under 35 USC 103(a)

The final Office Action rejected claims 7-12 under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Konno.

Applicant respectfully disagrees and traverses the above rejection as set forth below.

The combination of Kim's transmission circuits with Konno's capacitors is submitted to be improper because neither Kim nor Konno suggests such a combination and one skilled in the art would have no motivation to make such a combination.

Besides, even if the combination could be made, claim 7 distinguishes because the combination does not disclose, teach, or suggest, either implicitly or explicitly, all elements/features of claim 7.

In claim 7, the gate of the PMOS transistor is coupled with a ***reference*** voltage source, for example but not limited by, VDD/2. However, in Kim, the gate of the PMOS transistor T3 is coupled to a node D, and the potential of the node D is ***not fixed***. For example, in Kim's column 4 lines 49-50, the potential of the node D is pulled down by the switching circuit 15 in a case where the signal of the node C is logic high. Therefore, ***Kim does not disclose a PMOS transistor whose gate is coupled to a reference voltage source.***

Consequently, the combination of Kim in view of Konno does not render claim 7 obvious, and the rejection should be withdrawn.

Because independent claim 7 are allowable over the prior art of record, its dependent claim 8-14 are allowable as a matter of law, for at least the reason that the dependent claims contain all features/elements of their respectively independent claims.

Prior Art Made of Record

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

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CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-14 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,

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